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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Shunpei Yamazaki et al.                      Art Unit : 2815  
Serial No. : 10/799,722                                      Examiner : Edward Wojciechowicz  
Filed : March 15, 2004  
Title : HYBRID CIRCUIT AND ELECTRONIC DEVICE USING SAME

**MAIL STOP AF**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicants request consideration of the references listed on the attached PTO-1449 form. Under 37 C.F.R. § 1.98 (a)(2)(ii), only copies of foreign patent documents and/or non-patent literature are enclosed. Copies of any listed U.S. patents or U.S. patent application publications can be provided upon request.

The cited references were cited by the Japanese Patent Office in prosecution of a counterpart Japanese application in an office action dated August 23, 2005. That office action stated the following:

The "ceramic multi-layer substrate" described in paragraphs [0008] – [0020] and Fig. 1 of JP06-209168 is different from the present invention except that it fails to teach "a thin film transistor" and a function for treating "a high frequency." However, JP07-045787 teaches a "thin film transistor" as "a transistor" to be formed on a ceramic substrate. Also, JP57-133698 teaches the use of a circuit laminated on a ceramic substrate for a high frequency wave region. Further, since JP06-209168, JP07-045787 and JP57-133698 belong to the technical fields related to each other, it would have been easily achieved/conceived by those of ordinary skill in the art to employ "a thin film transistor" as a "transistor" for the use in a high frequency wave region when implementing the invention of JP06-209168 based on the teachings of JP07-045787 or JP57-133698.

It was well known to provide a film having a function of a heat radiator for a circuit over a ceramic substrate as shown in JP06-132421. It would have been obvious to

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employ this well known technique in the invention described in JP06-209168, JP07-045787 and JP57-133698.

This statement is being filed after a Notice of Allowance, but before payment of the issue fee. Each item of information in this statement (i) was cited in a communication from a foreign patent office in a counterpart foreign application, the communication being dated August 23, 2005, which is not more than three months prior to the filing of this statement, and (ii) was not first cited in any communication from a foreign patent office in a counterpart application which was more than three months prior to the filing date of this statement. A check for \$180 in payment of the late submission fee of §1.17(p) is enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 9/27/05

  
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John F. Hayden  
Reg. No. 37,640

**Customer No. 26171**  
Fish & Richardson P.C.  
1425 K Street, N.W. - 11th Floor  
Washington, DC 20005-3500  
Telephone: (202) 783-5070  
Facsimile: (202) 783-2331  
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Substitute Form PTO-1449 (Modified)  <b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 07977-221004	Application No. 10/799,722
	Applicant Shunpei Yamazaki et al.		
	Filing Date March 15, 2004	Group Art Unit 2815	

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	AL	JP57-133698	18 AUG 1982	JAPAN			FULL	
	AM	JP06-132421	13 MAY 1994	JAPAN			Abstract	
	AN	JP06-209168	26 JULY 1994	JAPAN			FULL	
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)		
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	AQ	
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Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	